REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

35 USC 112

Claims 4, 7 and 9 have been corrected to overcome the informalities noted by the Examiner.

Allowable subject matter

Applicant appreciates the Examiner's indication of allowable subject matter in claim 15.

Prior Art Rejections

Claims 1-10 were rejected under 35 USC 103(a) as being unpatentable over Sunahara (US Patent 6,153,290) in view of Ehman et al (US Patent No. 6,021,050). This ground of rejection is respectfully traversed. The combined teachings of these references do not suggest our claimed combinations.

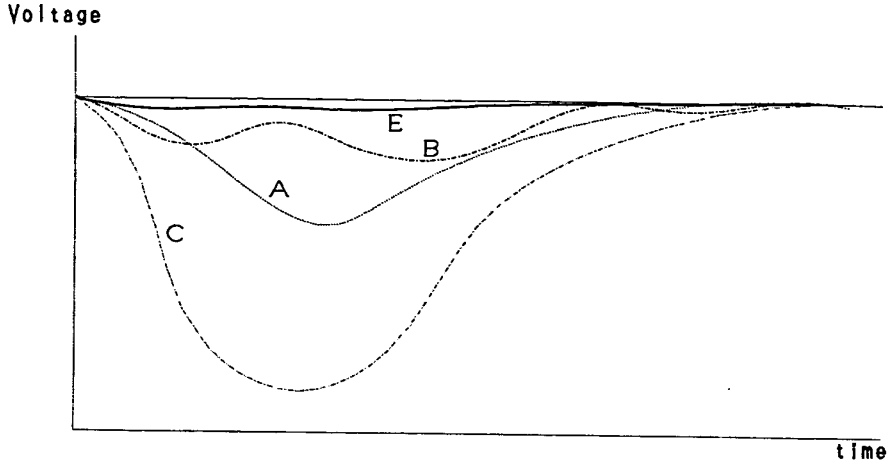
Our claimed combinations include, among others, the following two structural features:

1. the "capacitor is accommodated", and
2. the capacitor is located immediately below the IC chip.

Inclusion of a capacitor

The Examiner is referred to our specification at page 49 line 22 to page 50 line 7, which refers to Figure 12, reproduced below.

12/53
Fig. 12



The specification states:

> "Fig. 12 is a graph with a vertical axis indicating voltage supplied to the IC chip and a horizontal axis indicating time. In Fig. 12, two-dot chain line C denotes the voltage variation of a printed circuit board which is not provided with power supply capacitors. If power supply capacitors are not provided, voltage attenuates greatly. A broken line A denotes the voltage variation of a printed circuit board having chip capacitors mounted on the surfaces thereof. Compared with the two-dot chain line C, voltage does not drop greatly. However, since loop length is larger, rate-controlled power supply cannot be conducted sufficiently. Namely, at the start of the supply of power, voltage falls. Further, a two-dot chain line B denotes the voltage drop of a printed circuit board including the chip capacitors described above with reference to Fig. 8. In this case, loop length can be shortened; however, mass storage chip capacitors cannot be contained in a core substrate 30 and voltage, therefore, varies."

As mentioned in our specification at page 118 lines 8 to 15, "In a case where eight capacitors are connected in parallel:

Embedded type 60 pH

Reverse side mounted type72 pH

As can be understood from the above, it is possible to reduce inductance by including the chip capacitor (s) regardless of whether a single capacitor is used or capacitors are connected in parallel so as to increase storage capacity. "

Capacitor located immediately below IC chip

When the chip capacitor is placed immediately below the IC chip. The distance from the IC chip to each capacitor is shortened, and therefore, electric power can be instantaneously supplied to the IC chip. That is, the loop length which determines the loop inductance can be shortened.

The Sunahara reference shows the ceramic substrate including a plurality of capacitors, however does not show and suggest the circuit board for mounting an IC chip. That is, as shown in Fig. 3, the sheet-like support 48, 49 formed of ceramics are mounted on external terminal conductors (outmost layer) 19a, 19b. Sunahara does not mount the IC chip.

The Ehman reference shows a printed circuit board having a plurality of passive elements including capacitor. In column 5 lines 49 to 51 , "the passive components or other components 58 and 60 mounted on the top surface of the printed circuit board". Ehman, however, does not suggest that the "the capacitor located immediately below the IC chip."

In Ehman, since the passive elements including capacitor do not meet each other, it is not considered to shorten the distance between the IC chip and the capacitor. Therefore, it can not obtain the effect of "the loop length which determines the loop inductance can be shortened." in the present invention.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

Pillsbury Winthrop LLP

By: _____

Glenn J. Perry
Reg. No.:28458
Tel. No.: (703) 905-2161
Fax No.: (703) 905-2500

GJP\jjg
1600 Tysons Boulevard
McLean, VA 22102
(703) 905-2000